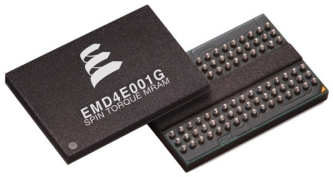
Everspin Releases Design Guide for using 1 Gb STT-MRAM with Xilinx DDR4 FPGA Controller

Everspin continues building ecosystem with strategic partnerships to bring 1 Gb STT-MRAM to the storage industry



Chandler, Ariz., Jan 21, 2020— Everspin Technologies, Inc. (NASDAQ: MRAM), the world's leading developer and manufacturer of Magnetoresistive RAM (MRAM), today announced a comprehensive design guide to streamline the integration of its 1 Gigabit (Gb) Spin-transfer Torque Magnetoresistive Random Access Memory (STT-MRAM) product in the storage market place. Xilinx, Inc., the leader in adaptive and intelligent computing, has been supporting Everspin's STT-MRAM for two generations and enables the 1 Gb STT-MRAM solution using its DDR4 controller in the Xilinx Vivado development environment.

The Everspin and Xilinx integrated solution provides many benefits, with the design guide and tools structured to address:

- Timing: Reducing operating frequency, increasing row access timing, increasing counter widths and reducing CAS page sizes
- Power-Up: Enabling anti-scribble mode during calibration
- Power-Down: Scramming or moving all relevant data into the persistent memory array
- Performance: Increasing pipeline depth and data transfer efficiency
- Scripts: Providing Verilog models and other detailed information to get storage OEM's design up and running effectively

"MRAM and persistent memory is an increasingly important technology across a broad range of solutions," said Jamon Bowen, Planning and Storage Segment Director, Data Center Group, Xilinx. "We see many applications where advanced capabilities like power loss protection is critical. It's exciting to see partners like Everspin make it easy for customers to develop world-class memory sub-systems leveraging the Xilinx platform."

Everspin's STT-MRAM devices allow enterprise infrastructure and data center providers to increase the reliability and performance of systems where high-performance data persistence is critical. This is achieved by delivering protection against power loss without the use of supercapacitors or batteries. In addition, the larger density 1 Gb part offers more effective management of I/O

streams, creating a greater level of latency determinism and allowing storage OEMs to significantly improve quality of service of their products. Similar benefits can also be achieved using the 1 Gb STT-MRAM device as a persistent data write buffer in storage and fabric accelerators, computational storage, and other applications.

“We value our partnership with Xilinx and continue to collaborate with them to bring our STT-MRAM solutions to market,” said Troy Winslow, Vice President of Sales and Marketing for Everspin. “Providing this design guide and tools will help streamline integration and time to market for our customers in providing enhanced applications for data centers.”

Additional Resources

- Everspin ST-DDR4 Design Guide for Xilinx FPGA Controllers
- Everspin Builds Ecosystem for 1-Gigabit Spin-transfer Torque Magnetoresistive Random Access Memory (STT-MRAM)
- Everspin Achieves Data Center OEM qualification of its 1Gb STT-MRAM Solution
- Everspin Blog

About Everspin Technologies

Everspin Technologies, Inc. is the world’s leading provider of Magnetoresistive RAM (MRAM), delivering unprecedented performance, non-volatility, endurance and reliability for applications where data persistence is paramount. Headquartered in Chandler, Arizona, Everspin is transforming the memory market with the largest and most diverse foundation of MRAM customers. For more information, visit www.everspin.com. NASDAQ: MRAM.

Cautionary Statement Regarding Forward-Looking Statements

This press release contains forward-looking statements regarding future events that involve risks and uncertainties that could cause actual results or events to differ materially from the expectations disclosed in the forward-looking statement, including, but not limited to; the anticipated market adoption of Everspin’s products and technology at the rate Everspin expects; the ability for Everspin to expand the markets Everspin addresses at the rate it expects; the risk that unexpected technical difficulties may develop in the final stages of development or production of its products, or when Everspin’s customers may ship in volume. Readers are advised that they should not place undue reliance on these forward-looking statements and should review the risk factors included in Everspin’s Form 10-Q filed with the Securities and Exchange Commission on Nov 7, 2019, under the caption “Risk Factors.” Subsequent events may cause these expectations to change, and Everspin disclaims any obligations to update or alter these forward-looking statements in the future, whether as a result of new information, future events or otherwise.

Everspin Contacts:
Rainier Communications
Marianne Sabella Dempsey/Joanne Stanway
617-223-8675/978-273-1473
everspin@rainierco.com